



Influence of triple-well technology on laser fault injection and laser sensor efficiency

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Speaker: Nicolas BORREL

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- **Context**

- Security robustness comparison in **dual**-well & **triple**-well architecture

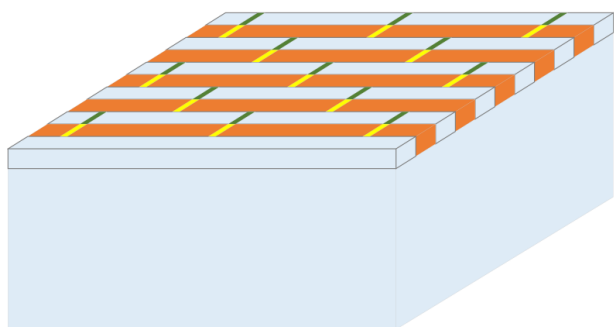
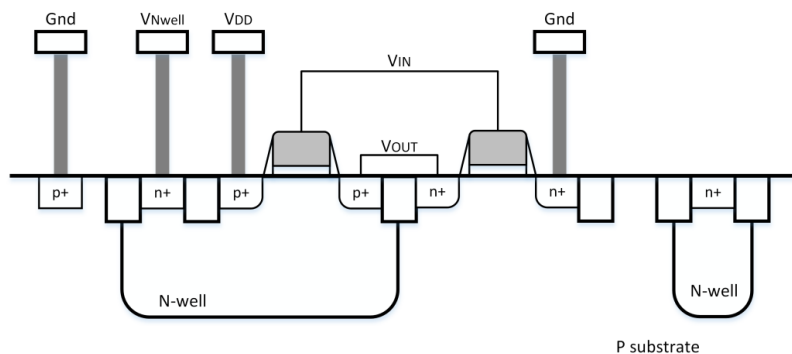
- **Objectives**

- Laser fault injection limit on **Flip-Flops**
- Laser **sensor** efficiency

- **Presentation**

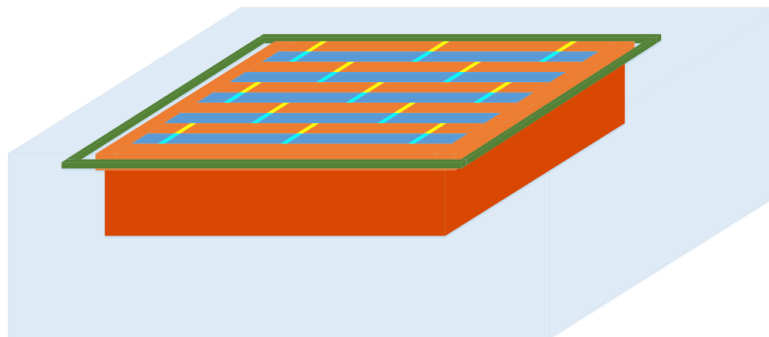
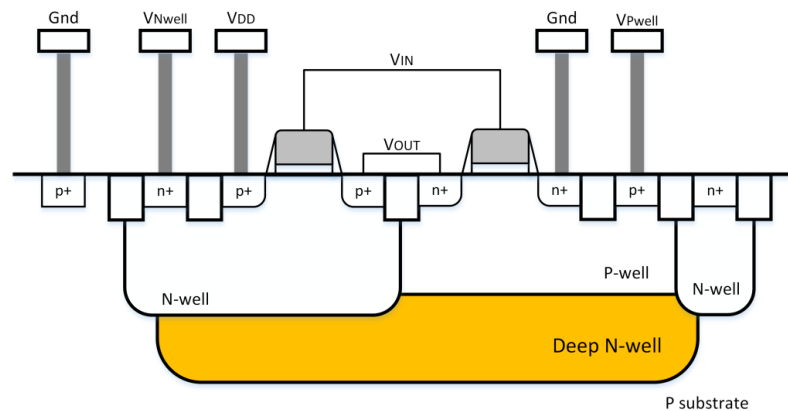
- Architecture
- Laser Fault Injection
- BBICS sensor
- BBICS optimization with the use of Body-Biasing

• Dual-well



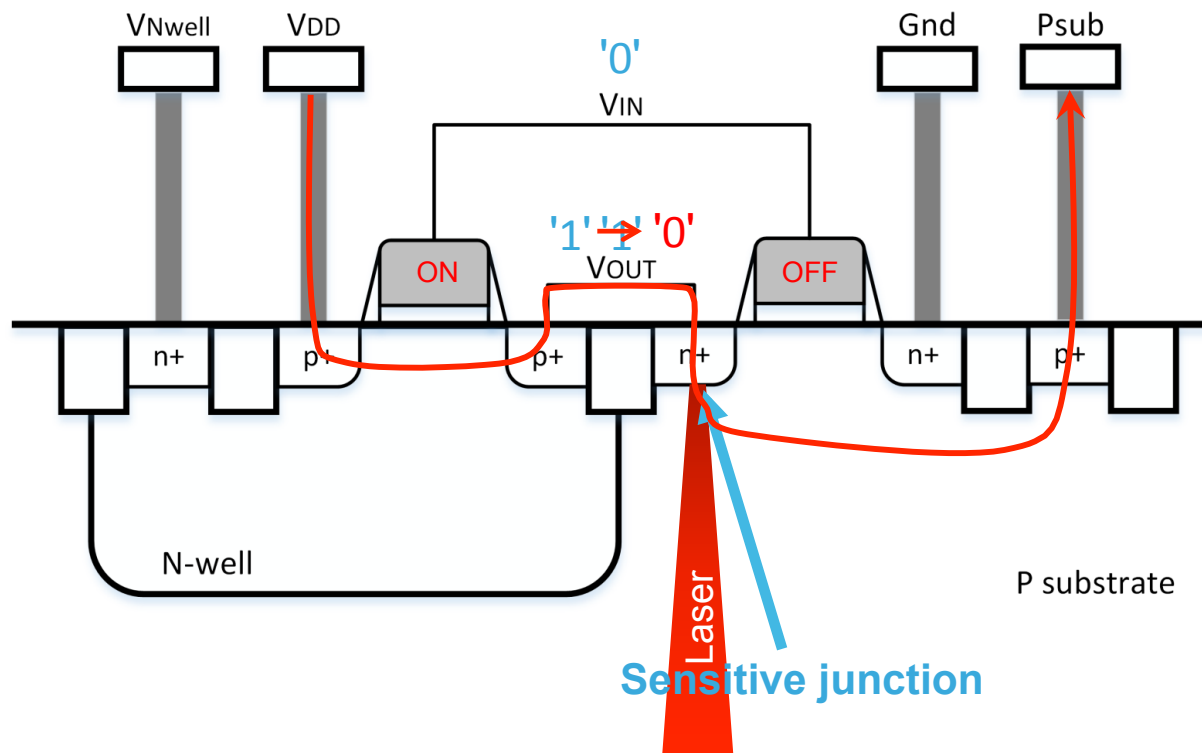
Nwell
 Psub
 Nwell Tap
 Psub Tap

• Triple-well



Nwell
 Deep-Nwell
 Pwell
 Psub
 Nwell Tap
 Pwell Tap
 Psub Tap

Laser Fault Injection principles



- **Bit reset: output from '1' to '0'**

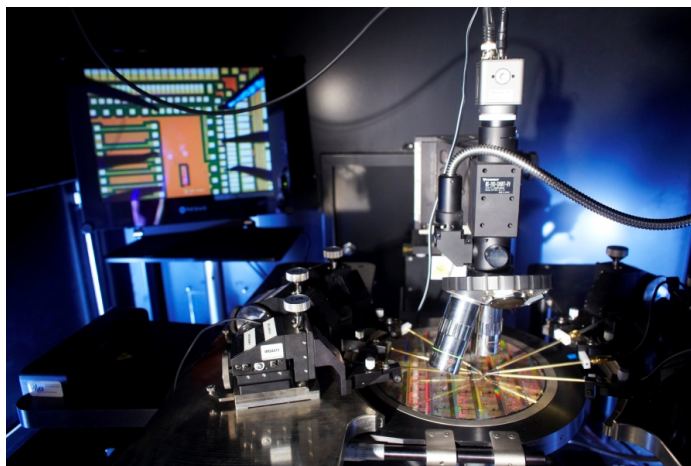
➤ Sensitive part: Drain of the NMOS

• Laser

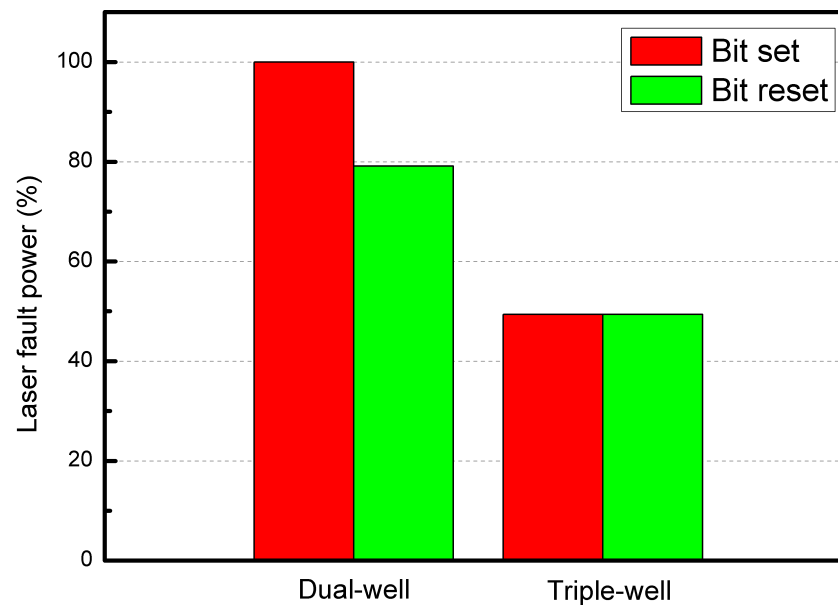
- Wavelength: 1064nm
- Pulse duration: 5μs
- Spot size: 1μm

• Device Under Test

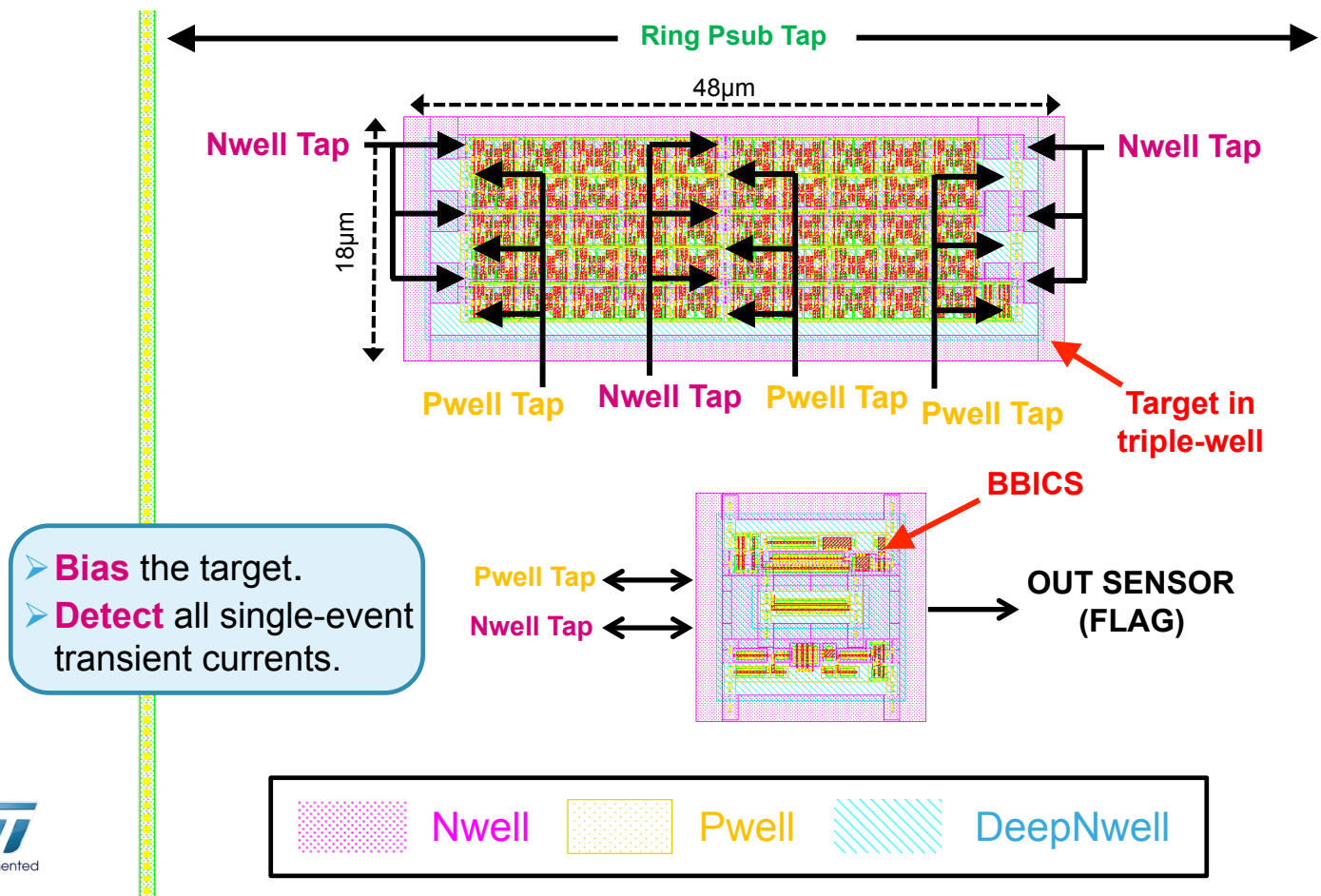
- CMOS 40nm STMicroelectronics
- Wafer thickness: 140μm



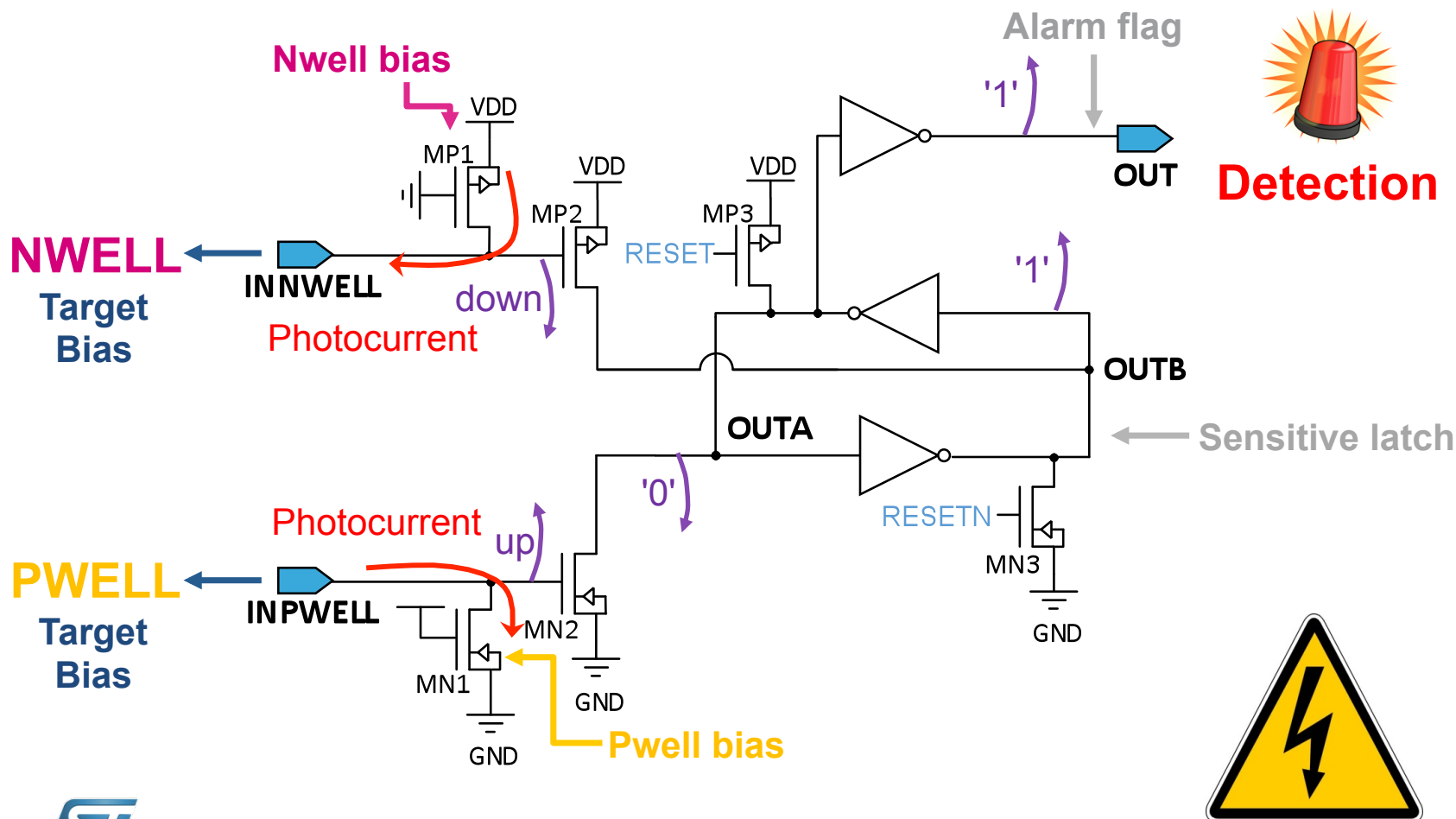
Flip-flop robustness evaluation



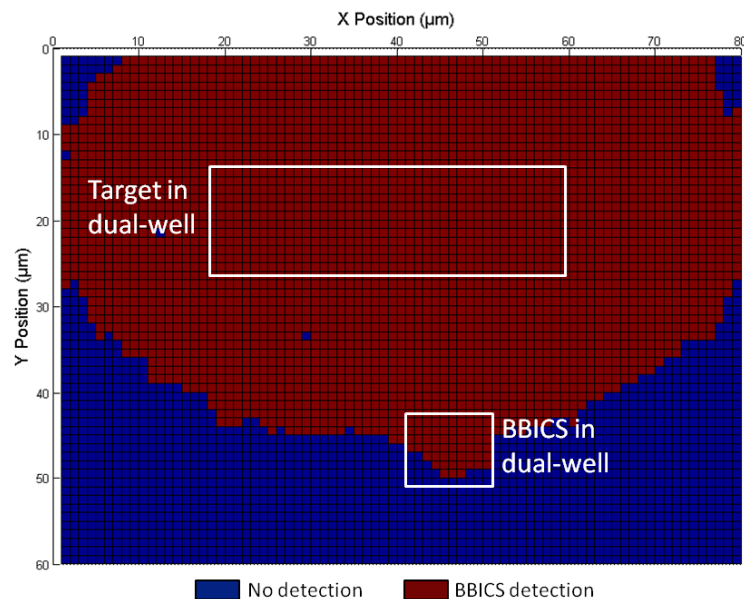
- **BBICS: Bulk Built-In Current Sensor**



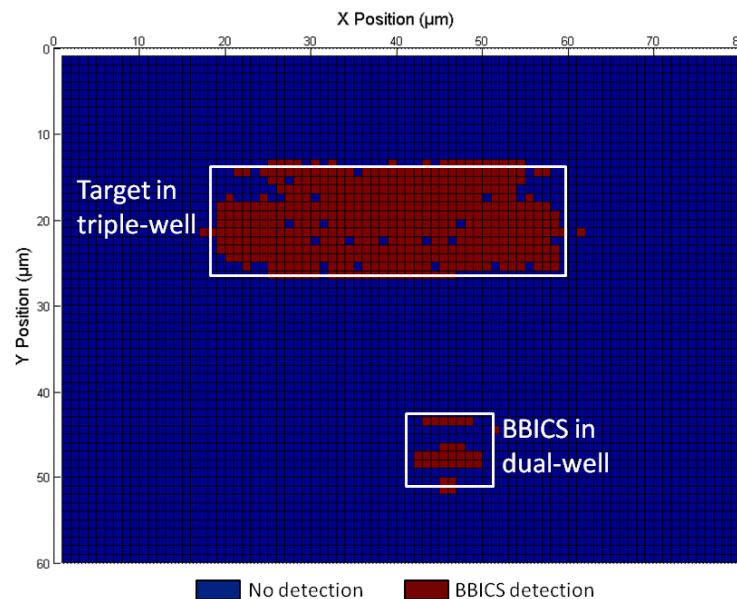
Architecture of BBICS



• Dual-well



• Triple-well

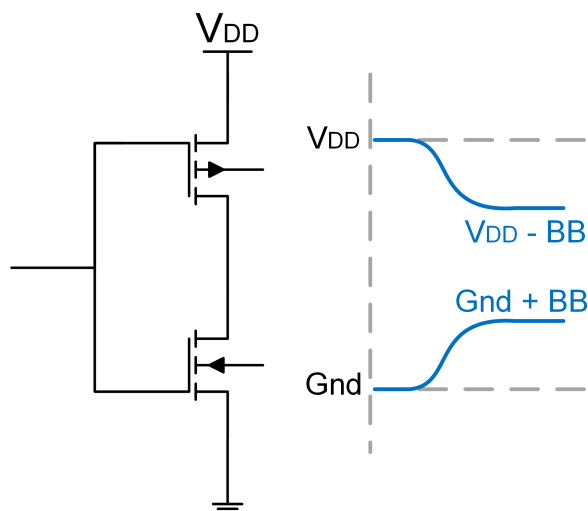


• BBICS coverage

➤ Dual-well >> Triple-well

The use of Body-biasing

• Low power Body-biasing techniques

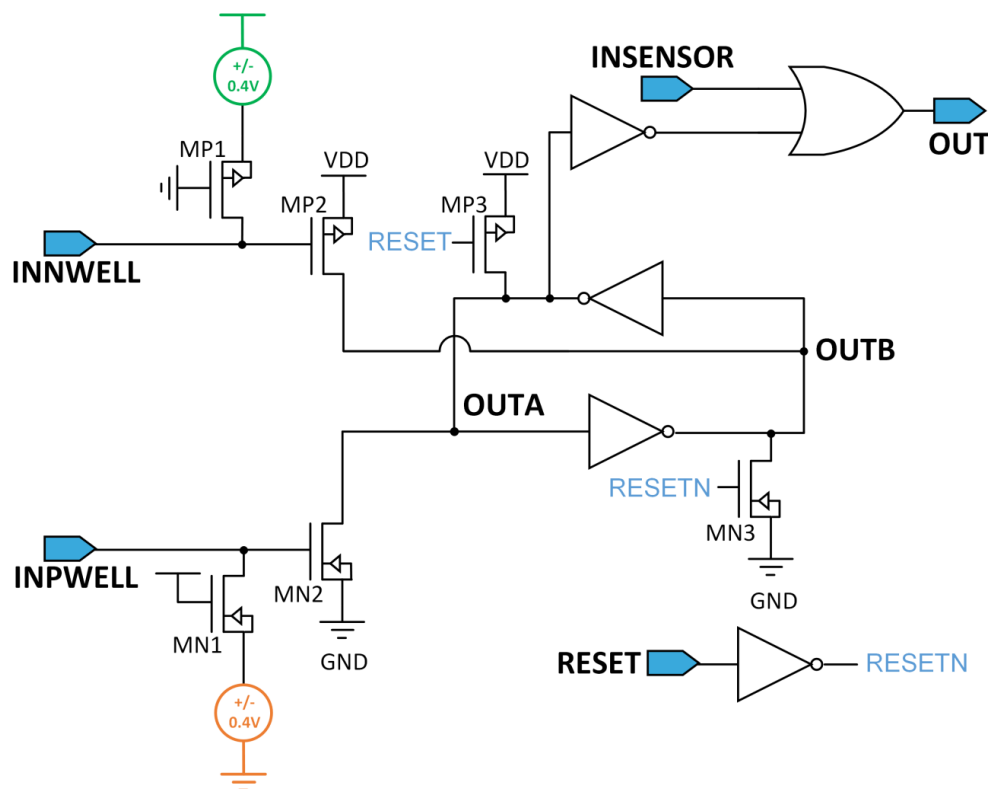


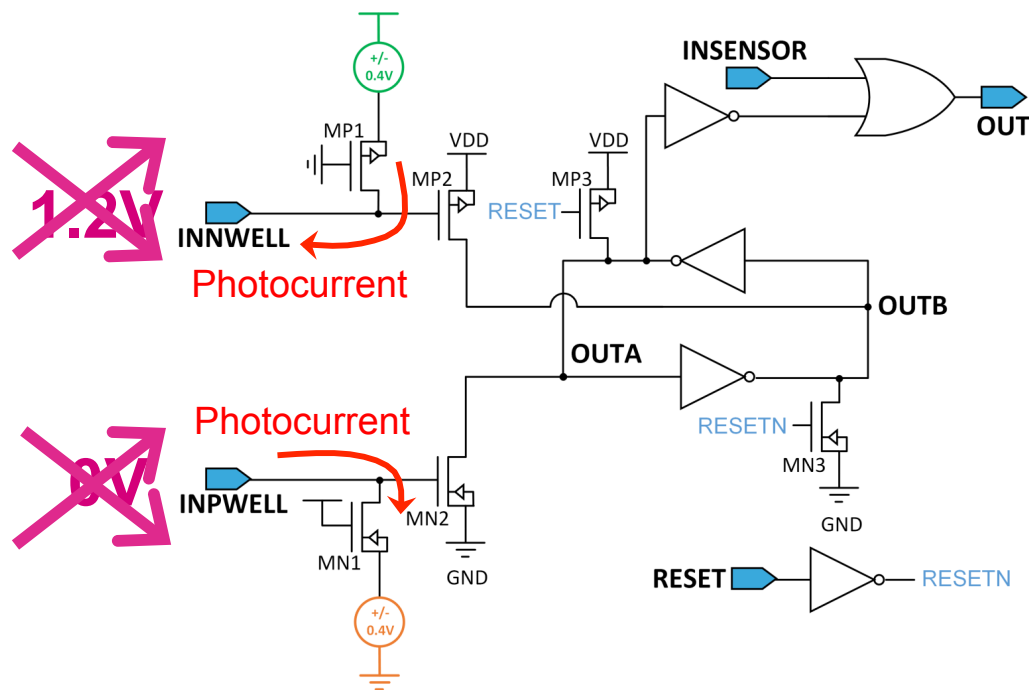
➤ Reverse Body-Biasing

➤ V_{th}

➤ Power consumption

• BBICS with Body-biasing architecture





Body-biasing	Nwell potential (V)	Pwell potential (V)	DeepNwell Current (μA)	Pwell current (μA)	Laser power (%)
RBB					
No BB					
FBB		-	- -	-	

- **Results comparison**

- Security Gate robustness architecture

Dual-well: **100%** >> triple-well: **50%**

- BBICS limit detection

Dual-well: **30%** << triple-well: **100%**



- BBICS with Body-biasing

triple-well: **15%**

- **Perspective**

- Silicon evaluation of BBICS with Body-biasing

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Thank you for your attention...
Q & A

Speaker: Nicolas BORREL

defect **&** in VLSI and
fault nanotechnology
tolerance systems

